Crossbow

Imote2 Hardware Reference Manual

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www.xbow.com

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About This Document

The following annotations have been used to provide additional information.

◀ NOTE

Note provides additional information about the topic.

☑ EXAMPLE

Examples are given throughout the manual to help the reader understand the terminology.

☞ IMPORTANT

This symbol defines items that have significant meaning to the user

⚠ WARNING

The user should pay particular attention to this symbol. It means there is a chance that physical harm could happen to either the person or the equipment.

The following paragraph heading formatting is used in this manual:

1 Heading 1

1.1 Heading 2

1.1.1 Heading 3

This document also uses different body text fonts (listed in Table 0-1) to help you distinguish between names of files, commands to be typed, and output coming from the computer.

Table 0-1. Font types used in this document.

Font Type	Usage
Courier New Normal	Sample code and screen output
Courier New Bold	Commands to be typed by the user
Times New Roman Italic	TinyOS files names, directory names
Franklin Medium Condensed	Text labels in GUIs

1 Introduction

This *User's Manual* describes the hardware features of the Imote2 Processor Radio (IPR2400) board and basic sensor board (ITS400).

Table 1-1 below lists the models covered in this Manual.

Table 1-1. Imote2 Models covered in the Reference Manual

Model Number	Description
IPR2400	Imote2 processor radio board
ITS400	Imote2 basic sensor board

This *Manual* is **not** a software guide to programming the Imote2, nor is it a guide to pre-built software packages that run on top of the Motes. The following resources are available regarding software:

Imote2.Builder SDK Manual by Crossbow Technology, Inc.

Imote2 Yahoo Users group at

> *http://tech.groups.yahoo.com/group/intel-mote2-community/*

Intel Imote2 resources page at

> http://www.intel.com/research/sensornets/

2 Imote2 Radio Processor Board (IPR2400)

The Crossbow Imote2 is an advanced sensor network node platform designed for demanding wireless sensor network applications requiring high CPU/DSP and wireless link performance and reliability. The platform is built around Intel's XScale® processor, PXA271. It integrates an 802.15.4 radio (TI CC2420) with an on-board antenna. It exposes a "basic sensor board" interface, consisting of two connectors on one side of the board, and an "advanced sensor board" interface, consisting of two high density connectors on the other side of the board. The Imote2 is a modular stackable platform and can be stacked with sensor boards to customize the system to a specific application, along with a "battery board" to supply power to the system.
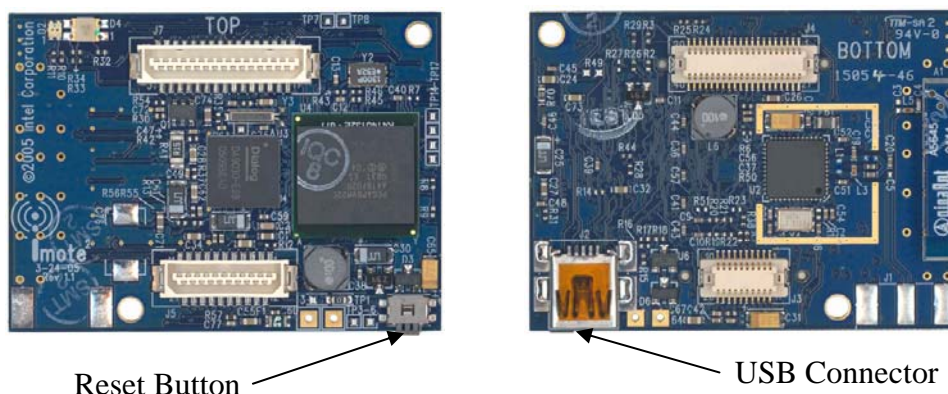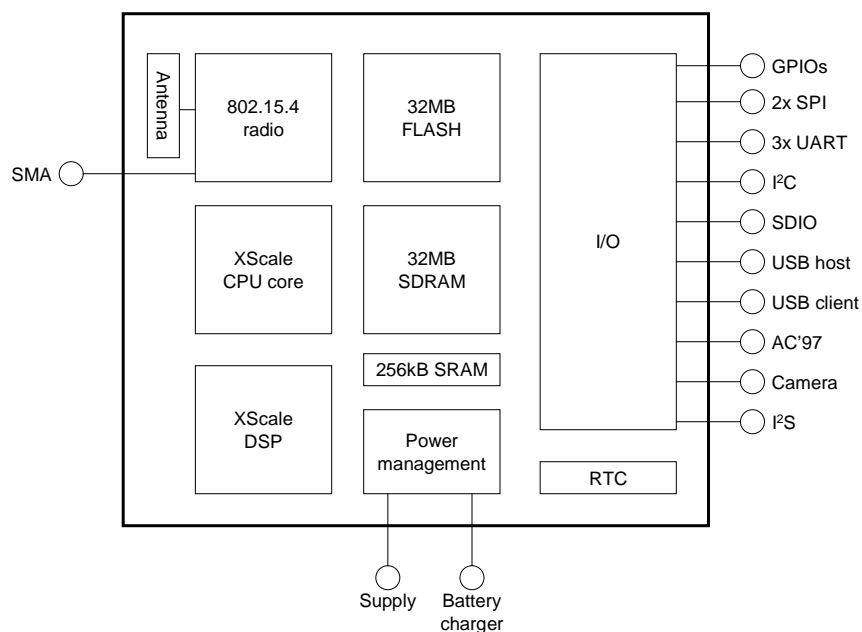

Figure 2-1. Photos of the Imote2 Board

Figure 2-2. Imote2 Block diagram

2.1 Features

- PXA271 XScale® processor @ [13–416] MHz
- Wireless MMX coprocessor
- 256kB SRAM, 32MB FLASH, 32MB SDRAM
- Integrated 802.15.4 radio, support for external radios through SDIO and UART
- Integrated 2.4GHz antenna
- Multicolor status indicator LED
- Basic and advanced expansion connectors supporting : 3xUART, I2C, 2xSPI, SDIO, I2S, AC97, USB host, Camera I/F, GPIO
- Mini-USB port for direct PC connection
- Size: 48 mm x 36 mm. PCB Thickness 1.75 mm

Table 2-1. Imote2 Operating Specifications

Parameter	Operating Value
Supply Voltage (V_{bat})	5.5 V
Charger Input Voltage (V_{chg})	10 V
Input Voltage (V_{in})	$V_{CC\,io} \pm 0.3$ V
Storage Temperature	-40 to +125^0 C
Operating Temperature	0 to +85^0 C
Current in deep sleep mode	387 μA
Current in active mode (13 MHz, radio off)	31 mA
Current in active mode (13 MHz, radio Tx/Rx)	44 mA
Current in active mode (104 MHz, radio Tx/Rx)	66 mA

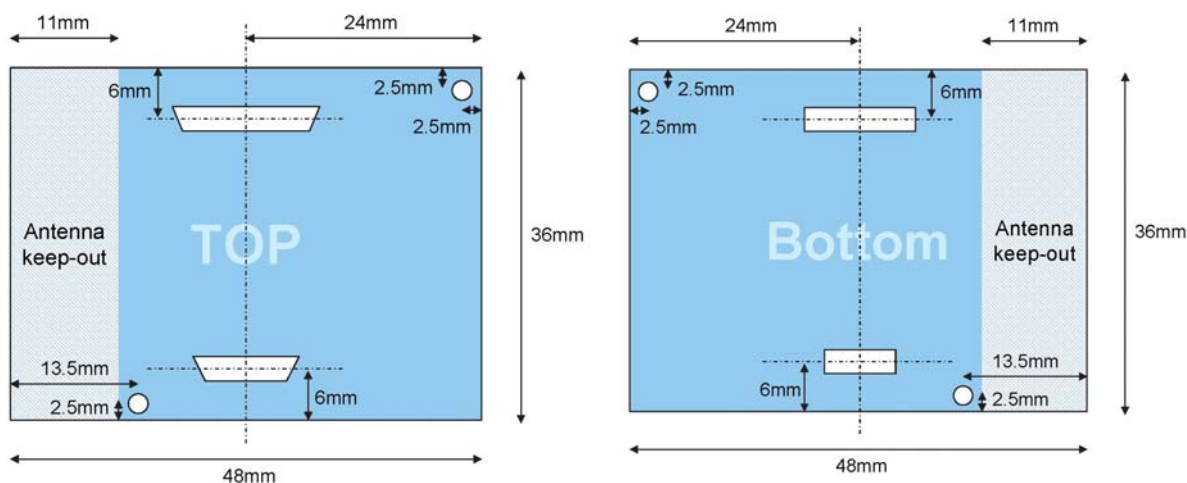## 2.2   Mechanical Dimensions

Figure 2-3. Mechanical Outline Drawing of OEM Edition Module

3 Processor

The Imote2 contains the PXA271 processor. This processor can operate in a low voltage (0.85V) and a low frequency (13 MHz) mode, hence enabling low power operation. The frequency can be scaled to 104 MHz at the lowest voltage level, and can be increased up to 416MHz with Dynamic Voltage Scaling. The processor has many low power modes, including sleep and deep sleep modes. It also integrates 256 KB of SRAM divided into 4 equal banks of 64 KB. The PXA271 is a multi-chip module that includes three chips in a single package, the processor, 32 MB SDRAM and 32 MB of flash. The processor integrates many I/O options making it extremely flexible in supporting different sensors, A/Ds, radio options, etc. These I/O options include I2C, 3 Synchronous Serial Ports one of which dedicated to the radio, 3 high speed UARTs, GPIOs, SDIO, USB client and host, AC97 and I2S audio codec interfaces, fast infrared port, PWM, Camera Interface and a high speed bus (Mobile Scaleable Link). The processor also adds many timers and a real time clock. The PXA271 also includes a wireless MMX coprocessor to accelerate multimedia operations. It adds 30 new media processor instructions, support for alignment and video operations and compatibility with Intel MMX and SSE integer instructions.

4 Radios and Antenna

4.1 Radio

The Imote2 integrates an 802.15.4 radio transceiver from ChipCon (CC2420). 802.15.4 is an IEEE standard describing the physical & MAC layers of a low power low range radio, aimed at control and monitoring applications. The CC2420 supports a 250 kb/s data rate with 16 channels in the 2.4 GHz band.

Other external radio modules such as 802.11 and Bluetooth can be enabled through the supported interfaces (SDIO, UART, SPI, etc).

4.1.1 Radio RF Channel Selection

The Imote2's CC2420 radio can be tuned within the IEEE 802.15.4 channels that are numbered from 11 (2.405 GHz) to 26 (2.480 GHz) each separated by 5 MHz.

4.1.2 Radio Transmission Power

RF transmission power is programmable from 0 dBm (1 mW) to –25dBm. Lower transmission power can be advantageous by reducing interference and dropping radio power consumption from 17.5 mA at full power to 8.5 mA at lowest power.

Table 4-1. Chipcon® CC2420 Output Power Settings and Typical Current Consumption

RF Power (dBm)	Power Register (code)	Current Consumption (mA)
0	31	17.4
-1	27	16.5
-3	23	15.2
-5	19	13.9
-7	15	12.5
-10	11	11.2
-15	7	9.9
-25	3	8.5

The RF received signal strength indication (RSSI) is read directly from the CC2420 Radio and sent with every radio packet received. Typical RSSI values for a given RF input level are shown in Figure 4-1 below.
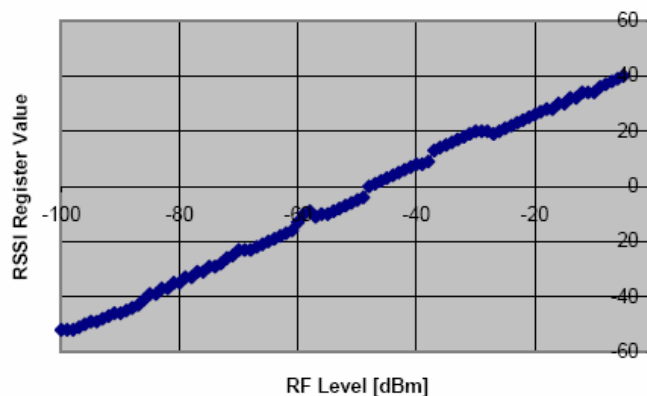
Figure 4-1. Typical RSSI value versus input RF level in dBm

4.2 Antenna

The Imote2 platform integrates a 2.4 GHz surface mount antenna which provides a nominal range of about 30 meters. If a longer range is desired, an SMA connector can be soldered directly to the board to connect to an external antenna.

There are literally hundreds of antenna options offered by different vendors and some references are provided below:

- Linx Technologies: http://www.linxtechnologies.com/
- Nearson: http://www.nearson.com/

5 Power

5.1 Power Supply Options

To supply the processor with all the required voltage domains, the Imote2 includes a Power Management IC. This PMIC supplies 9 voltage domains to the processor in addition to the Dynamic Voltage Scaling capability. It also includes a battery charging option and battery voltage monitoring. Two of the PMIC voltage regulators (1.8 V & 3.0 V) are used to supply the sensor boards with the desired regulated supplies at a maximum current of 200 mA. The processor communicates with the PMIC over a dedicated I2C bus (PWRI2C). The Imote2 platform was designed to support primary and rechargeable battery options as described below, in addition to being powered via USB. The following figure shows how the different battery boards and on board connectors can be used to power the mote.

5.1.1 Primary Battery

The Imote2 platform can be powered using primary batteries with a voltage range of 3.2 - 4.5 V (e.g. 3 AAA alkaline batteries). A battery board with a basic or advanced set of connectors can be connected to the Vbat pins of the connector. As shown in the figure below, a diode and fuse should be connected between the battery and mote board to protect the battery and the PMIC.

5.1.2 Rechargeable Battery

A rechargeable battery can be used to supply power to the Imote2 platform by connecting it directly to the Vbat pin on the connector. In this case, the PMIC battery charger can be used to recharge the batteries. The battery board should drive the nCHARGE_EN pin low to connect the USB input to the PMIC charger pin, hence allowing to recharge the battery using USB. The PMIC supports single cell Li-Ion at 4.1 and 4.2 V, in addition to a Li-Polymer pack. See the figure below for more details.

5.1.3 Mini-USB connector input

The mote can be powered directly from USB, by routing the USB power to the Vbat input of the PMIC. This is the default state when either a battery is not connected, or when a battery board drives the nCHARGE_EN input high (as the case with all primary battery boards). If a battery board pulls nCHARGE_EN low, the USB input gets routed to the Vchg pin of the PMIC, which would be the case for rechargeable batteries as mentioned above.

5.1.4 On-board pads

The On board pads can be used to connect a primary battery directly to the mote. A diode is included in this path to protect the primary battery. In addition, these pads can be used to connect any power source supplying a voltage range of 3.2 – 4.5V (after the diode drop). This connector is similar to the USB connector functionality, as it could be used to supply power to the mote or to recharge a battery based on the state of the nCHARGE_EN pin.

The PMIC is also used to enable the alarm functionality that is exposed on the basic and advanced sensor connectors. When power is supplied to the mote, the PMIC will start, however it will not start the mote until the power button is pushed (similar to a cell phone usage model).

If it is desired to have a power board automatically turn on the mote, the power board can short the alarm pin on the connector to the VRTC pin. This will cause the mote to start automatically every time power is applied to the mote. However, if a more intelligent sensor board is desired to start the mote in response to a specific sensor event, the alarm pin can be controlled by the sensor board to start/wakeup the mote selectively.
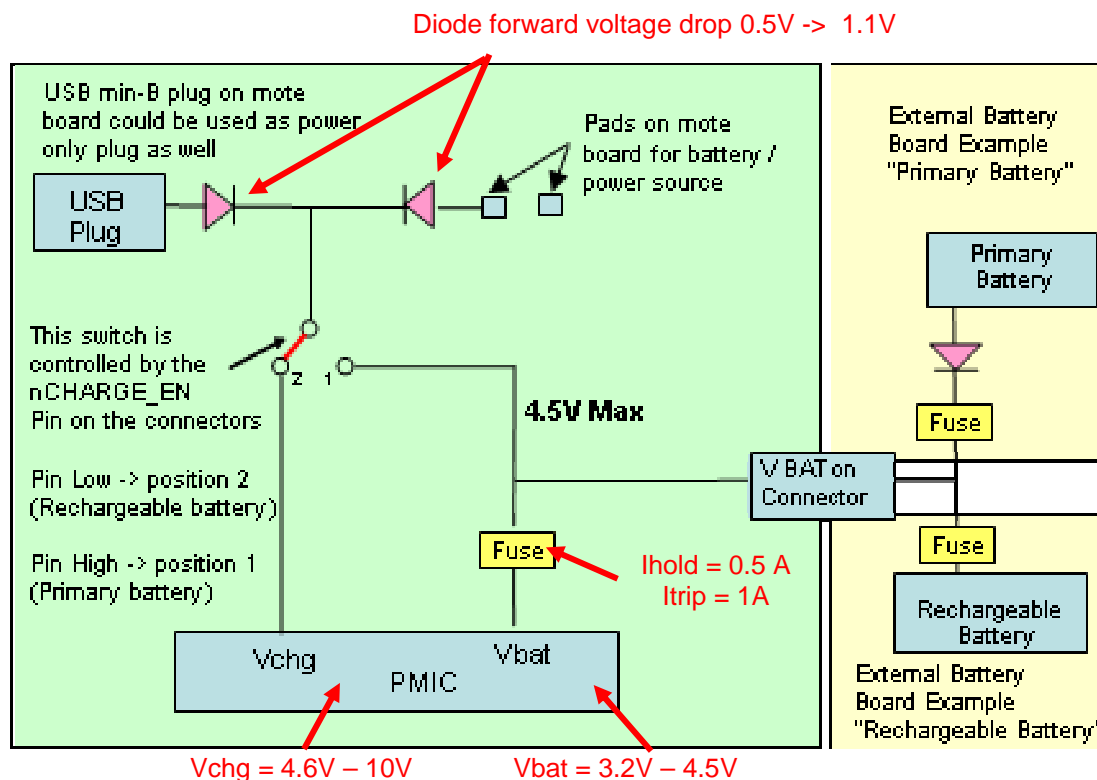

Figure 5-1. Power supply options for Imote2

6 Sensor Boards & Expansion Connectors

6.1 Sensor Board Interfaces

The Imote2 platform exposes two sets of connectors, the basic set and the advanced set. The pins on each connector set are split into two physical connectors to enhance the mechanical stability. The basic set is meant to enable low cost sensor boards (low density connectors were chosen) and support the most common sensor interfaces. This connector set is defined as the "architectural" set, and can be supported in future mote designs. The advanced connector set exposes some of the PXA271 advanced features (Camera Interface, High speed bus, Audio interfaces, etc), and is assumed to be platform specific. The details of the connector sets are described below.
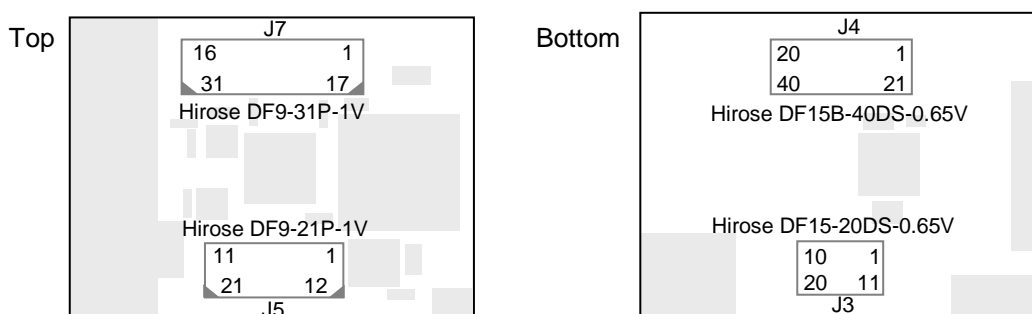

Figure 6-1. Connector information for Imote2

Table 6-1. Matching connector information

Description	Manufacturer	Part#
40 pin (J4)	Hirose	DF15B(3.2)-40DP-0.65V
20 pin (J3)	Hirose	DF15B(3.2)-20DP-0.65V
31 pin (J1)	Hirose	DF9-31S-1V
21 pin (J5)	Hirose	DF9-21S-1V

◄ **NOTE:** The Hirose DF15 connector type comes in wide variety of stacking heights. Using the recommended part numbers will result in a 5mm stacking height on the bottom side. If desired, an expansion board designer can choose a different part number of the DF15 connector used in order to meet custom stacking height requirements.

6.1.1 Basic Connector Set

The basic connector set consists of 2 physical connectors from the Hirose DF9 family which has a 1 mm pitch. The connector choice simplifies the routing and soldering of sensor boards, which is useful in the prototyping stage. The pins are split between the 2 connectors (31 pin and 21 pin connectors) for mechanical stability reasons. The asymmetry of the two connectors provides a useful visual clue of sensor board orientation. All I/O pins can be programmed as GPIOs in addition to their special port function. As mentioned in the power supply section, the 1.8 and 3.0

V pins are supplied by the PMIC and can be used to power the sensor boards. The alarm pin is an input pin and can be used by the sensor boards to wake up the processor out of deep sleep mode if needed. The reset pin is an input pin to force a hardware reset of the processor. The standard UART will be used as the debug console and is exposed on the 21 pin connector. The 31 pin connector exposes 2 high speed UART ports, 2 SSP ports, an SDIO port, an I2C port and multiple GPIOs. There are 11 reserved pins to allow for future expansion and inter-board communication.
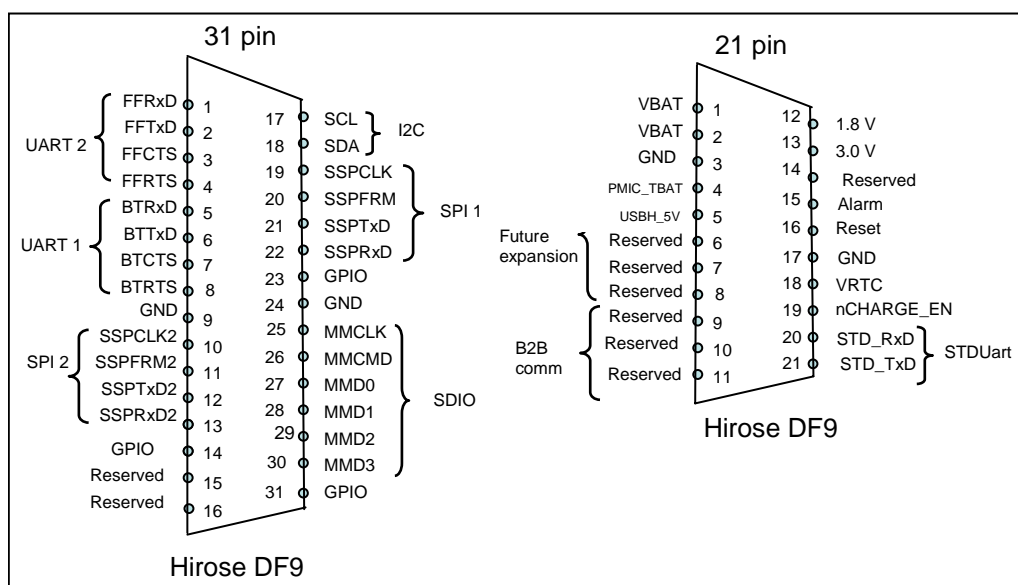

Table 6-2. Pin-out description for basic large connector (J7)

Pin#	Type	Name	GPIO#	Description
1	I/O	FF_RXD	96	UART 1 receive data
2	I/O	FF_TXD	99	UART 1 send data
3	I/O	FF_CTS	100	UART 1 clear to send
4	I/O	FF_RTS	98	UART 1 request to send
5	I/O	BT_RXD	42	UART 2 receive data
6	I/O	BT_TXD	43	UART 2 send data
7	I/O	BT_CTS	44	UART 2 clear to send
8	I/O	BT_RTS	45	UART 2 request to send
9		GND		Ground
10	I/O	SSP2_SCLK	36	Synchronous Serial Port 2 clock
11	I/O	SSP2_SFRM	37	Synchronous Serial Port 2 frame
12	I/O	SSP2_TXD	38	Synchronous Serial Port 2 transmit data
13	I/O	SSP2_RXD	11	Synchronous Serial Port 2 receive data
14	I/O	GPIO94	94	General purpose I/O
15	R	Reserved		Do not connect
16	R	Reserved		Do not connect
17	I/O	I2C_SCL	117	I2C serial clock
18	I/O	I2C_SDA	118	I2C serial data/address bus
19	I/O	SSP1_SCLK	23	Synchronous Serial Port 1 clock
20	I/O	SSP1_SFRM	24	Synchronous Serial Port 1 frame
21	I/O	SSP1_TXD	25	Synchronous Serial Port 1 transmit data
22	I/O	SSP1_RXD	26	Synchronous Serial Port 1 receive data
23	I/O	GPIO10	10	General purpose I/O
24		GND		Ground
25	I/O	MM_CLK	32	MMC and SD/SDIO bus clock

26	I/O	MM_CMD	112	MMC and SD/SDIO command
27	I/O	MM_DAT0	92	MMC and SD/SDIO read / write data 0
28	I/O	MM_DAT1	109	MMC and SD/SDIO read / write data 1
29	I/O	MM_DAT2	110	MMC chip select 0 or SD/SDIO read / write data 2
30	I/O	MM_DAT3	111	MMC chip select 1 or SD/SDIO read / write data 3
31	I/O	GPIO93	93	General purpose I/O

Table 6-3. Pin-out description for basic small connector (J5)

Pin#	Type	Name	GPIO#	Description
1		VBAT		Power Supply Rail (3.2 – 4.7 V minus Diode Drop)
2		VBAT		Power Supply Rail (3.2 – 4.7 V minus Diode Drop)
3		GND		Ground
4	I	PMIC_TBAT		Battery temperature input
5		USBH_5V		5.0 V supply rail to power sensor board (USBH)
6	R	Reserved		Do not connect
7	R	Reserved		Do not connect
8	R	Reserved		Do not connect
9	R	N/C		Available for communication between expansion boards
10	R	N/C		Available for communication between expansion boards
11	R	N/C		Available for communication between expansion boards
12		VCC_1P8		1.8 V supply rail to power sensor boards
13		VCC_3V		3.0 V supply rail to power sensor boards
14	R	Reserved		Do not connect
15	I	ALARM		Alarm input to PMIC (see power subsystem)
16	O	NRESET		Processor reset
17		GND		Ground
18		VCC_RTC		Power supply for the RTC voltage domain of the PXA
19	I	nCHARGE_EN		Battery select, 0 : rechargeable battery, 1 : primary battery
20	I/O	STD_RXD	46	UART 3 receive data
21	I/O	STD_TXD	47	UART 3 send data

6.1.2 Advanced Connector Set

The advanced connector set also consists of 2 physical connectors. We chose a higher density connector (0.65mm pitch) for the advanced set to be able to support the large pin count required without increasing the size of the connector too much. The pins are split on 2 connectors (40 pin and 20 pin connectors) for mechanical stability reasons. Note that all I/O pins (with the exception of JTAG and USB) can be programmed as GPIOs in addition to their special port function. JTAG is exposed on the 20 pin connector. The MSL interface provides two independent high speed unidirectional links. The data-channel width can be scaled from 1 to 4 bits, providing up to 192 Mbps at 48 MHz. The CIF port supports the Intel Quick Capture Camera Interface, to easily attach image sensors to the Imote2. Note that the I^{2}C, UART and SPI ports exposed on the 40 pin connector, are the same ports exposed on the basic side.
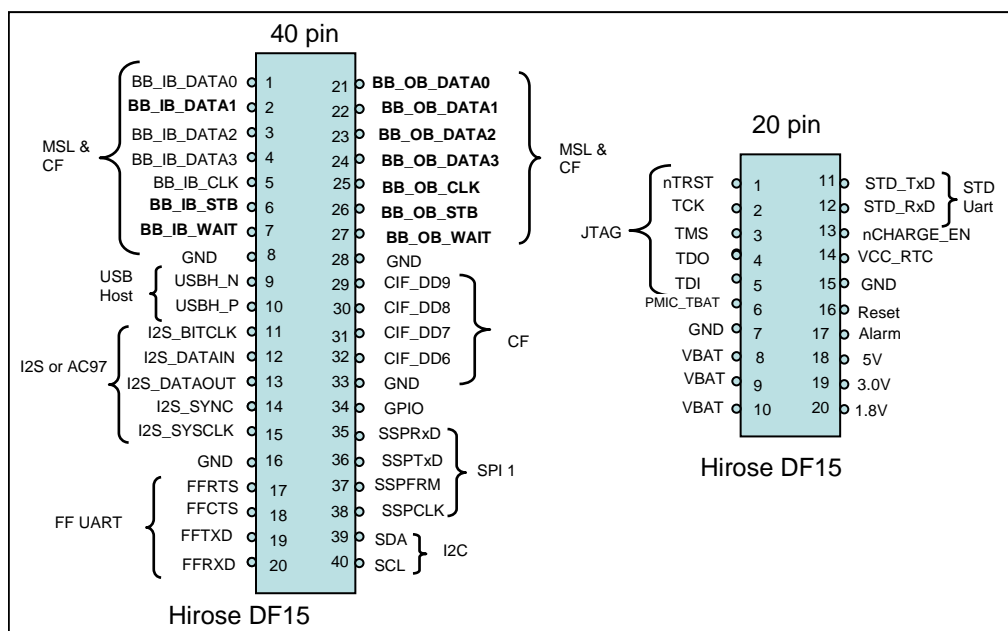
Table 6-4. Pin-out description for advanced large connector (J4)

Pin#	Type	Name	GPIO#	Description
1	I/O	BB_IB_DATA0 CIF_DD5	82	MSL inbound data bit 0 Quick capture data line 5
2	I/O	BB_IB_DATA1 CIF_DD1	55	MSL inbound data bit 1 Quick capture data line 1
3	I/O	BB_IB_DATA2	56	MSL inbound data bit 2
4	I/O	BB_IB_DATA3	57	MSL inbound data bit 3
5	I/O	BB_IB_CLK CIF_DD4	83	MSL inbound clock strobe Quick capture data line 4
6	I/O	BB_IB_STB CIF_FV	84	MSL inbound signal qualifier Quick capture frame start
7	I/O	BB_IB_WAIT CIF_LV	85	MSL wait indicator for inbound link Quick capture line start
8		GND		Ground
9	I/O	USBH_N_CONN		Data negative differential signal (USB D-)
10	I/O	USBH_P_CONN		Data positive differential signal (USB D+)
11	I/O	I2S_BITCLK AC97_BITCLK	28	I2S bit clock, supplies the serial audio bit rate AC97 12.288-MHz bit-rate clock
12	I/O	I2S_DATA_IN AC97_SDATA_IN_0	29	I2S Serial audio input data from CODEC AC97 Serial audio input data from CODEC
13	I/O	I2S_DATA_OUT AC97_SDATA_OUT	30	I2S Serial audio output data to CODEC AC97 Serial audio output data to CODEC
14	I/O	I2S_SYNC AC97_SYNC	31	I2S SYNC, BITCLCK divided by 64 AC97 48-KHz frame indicator and synchronizer
15	I/O	I2S_SYSCLK AC97_RESET_n	113	I2S system clock = BITCLK x 4 AC97 CODEC reset
16		GND		Ground
17	I/O	FF_RTS	98	UART 1 request to send
18	I/O	FF_CTS	100	UART 1 clear to send
19	I/O	FF_TXD	99	UART 1 send data
20	I/O	FF_RXD	96	UART 1 receive data
21	I/O	BB_OB_DATA0 CIF_DD0	81	MSL outbound data bit 0 Quick capture data line 0
22	I/O	BB_OB_DATA1 CIF_DD5	48	MSL outbound data bit 1 Quick capture data line 5
23	I/O	BB_OB_DATA2 CIF_DD3	50	MSL outbound data bit 2 Quick capture data line 3

24	I/O	BB_OB_DATA3 CIF_DD2	51	MSL outbound data bit 3 Quick capture data line 2
25	I/O	BB_OB_CLK CIF_DD4	52	MSL outbound clock strobe Quick capture data line 4
26	I/O	BB_OB_STB CIF_MCLK	53	MSL outbound signal qualifier Quick capture programmable output clock
27	I/O	BB_OB_WAIT CIF_PCLK	54	MSL wait indicator for outbound link Quick capture pixel clock
28		GND		Ground
29	I/O	CIF_DD9	106	Quick capture data line 9
30	I/O	CIF_DD8	107	Quick capture data line 8
31	I/O	CIF_DD7	12	Quick capture data line 7
32	I/O	CIF_DD6	17	Quick capture data line 6
33		GND		Ground
34	I/O	GPIO10	10	General purpose I/O
35	I/O	SSP1_RXD	26	Synchronous Serial Port 1 receive data
36	I/O	SSP1_TXD	25	Synchronous Serial Port 1 transmit data
37	I/O	SSP1_SFRM	24	Synchronous Serial Port 1 frame
38	I/O	SSP1_SCLK	23	Synchronous Serial Port 1 clock
39	I/O	I2C_SDA	118	I2C serial data
40	I/O	I2C_SCL	117	I2C serial clock

Table 6-5. Pin-out description for advanced small connector (J3)

Pin#	Type	Name	GPIO#	Description
1	I	JTAG_NTRST		JTAG port : Test Reset
2	I	JTAG_TCK		JTAG port : Test clock
3	I	JTAG_TMS		JTAG port : Test mode select
4	O	JTAG_TDO		JTAG port : Test data out
5	I	JTAG_TDI		JTAG port : Test data in
6	I	PMIC_TBAT		Battery temperature input
7		GND		Ground
8		VBAT		Power Supply Rail (3.2 – 4.7 V minus Diode Drop)
9		VBAT		Power Supply Rail (3.2 – 4.7 V minus Diode Drop)
10		VBAT		Power Supply Rail (3.2 – 4.7 V minus Diode Drop)
11	I	STD_RXD		UART 3 receive data
12	O	STD_TXD		UART 3 send data
13	I	nCHARGE_EN		Battery select, 0 : rechargeable battery, 1 : primary battery
14		VCC_BAT_RTC		Power supply for the RTC voltage domain of the CPU
15		GND		Ground
16	O	NRESET		Processor reset
17	I	ALARM		Alarm input to PMIC (see power subsystem)
18		VCC_5V		5.0 V supply rail to power sensor board (USBH)
19		VCC_3V		3.0 V supply rail to power sensor boards
20		VCC_1P8		1.8 V supply rail to power sensor boards

Table 6-6. Imote2 Internal I/O configuration

Component	Pin name	GPIO#
LED	Red	103
LED	Green	104
LED	Blue	105
CC2420	FIFO	114
CC2420	VREG_EN	115
CC2420	CCA	116

CC2420	FIFOP	0
CC2420	RESETN	22
CC2420	SFD	16

Table 6-7. Imote2 Test Points

Test Point Name	Signal
TP3	PWR pad for direct battery connection
TP4	GND pad for direct battery connection
TP5	STD_TXD
TP6	STD_RXD
TP7	PWR_SCL
TP8	PWR_SDA
TP9	13 MHz to PMIC
TP14	PWR_EN
TP15	SYS_EN
TP16	NVDD_FAULT
TP17	NBATT_FAULT

7   ITS400 Basic Sensor Board

The basic sensor board is designed to connect to the basic connectors on the Imote2. It contains a 3d Accelerometer, advanced temp/humidity sensor, light sensor and 4 channel A/D. It is a pass through board to allow stacking with another sensor/communication board.
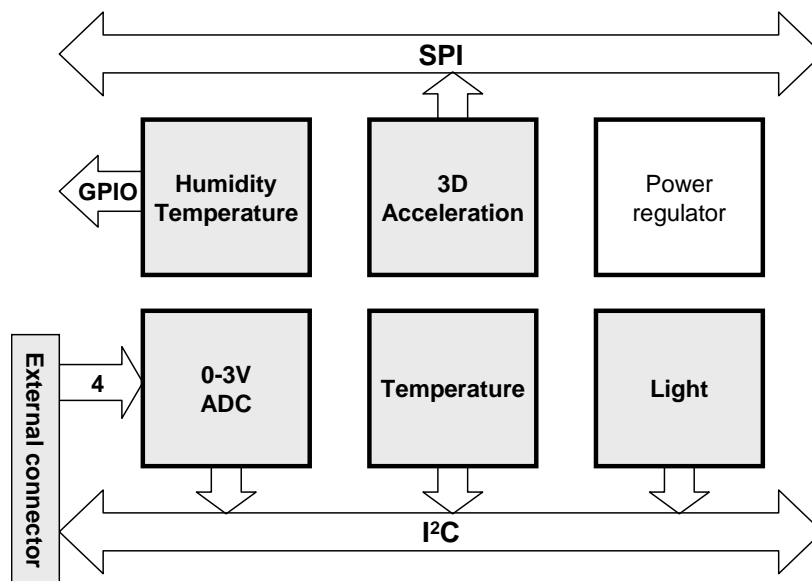
Figure 7-1. Photo of the ITS400 Sensor Board

Figure 7-2. ITS400 Block diagram

Table 7-1. ITS400 Operating Specifications

| Parameter	Operating Value
Operating temperature range	0 to +70 ºC
Storage temperature range	-40 to +150 ºC
Humidity (non condensing)	80 %

7.1 Sensor Suite

The ITS400 sensor board is multi-sensor board that combines a popular set of sensors for wireless sensor network applications, including:

- ST Micro LIS3L02DQ 3d 12 bit ±2g accelerometer
- High Accuracy, ±0.3°C Sensirion SHT15 temperature/humidity sensor
- TAOS TSL2651Light Sensor
- Maxim MAX1363 4 Channel General Purpose A/D for quick prototyping
- TI Tmp175 Digital Temperature Sensor with two-wire interface

7.1.1 3D Accelerometer

This board includes an ST Micro LIS3L02DQ 3d accelerometer. This sensor has a range of +/-2g with 12 bit resolution. It offers two possible interfaces, SPI or I2C, either of which is selectable using 0-ohm resistors including on the board. To communicate with the sensor using the I2C interface, populate R17 and remove R21. To communicate with the sensor using SPI, populate R21 and remove R17. By default, the sensor is connected to SSP1 on the Intel Mote 2. In the event that another stacked board conflicts with the basic sensor board use of SSP1, the sensor may be disconnected from the port by removing R23, R24, R25 and R26, and connected to SSP2 instead by populating R29, R30, R31, R32 with zero ohm resistors. The sensor's data ready (RDY_INT) interrupt is connected to GPIO96 through an OR gate as shown in the schematic below. If another board conflicts with the use of GPIO 96, the BT_RXD pin can be used instead by loading R34. For more info on this sensor, the datasheet can be found at http://www.stmicro.fr/stonline/products/literature/ds/10175.pdf.
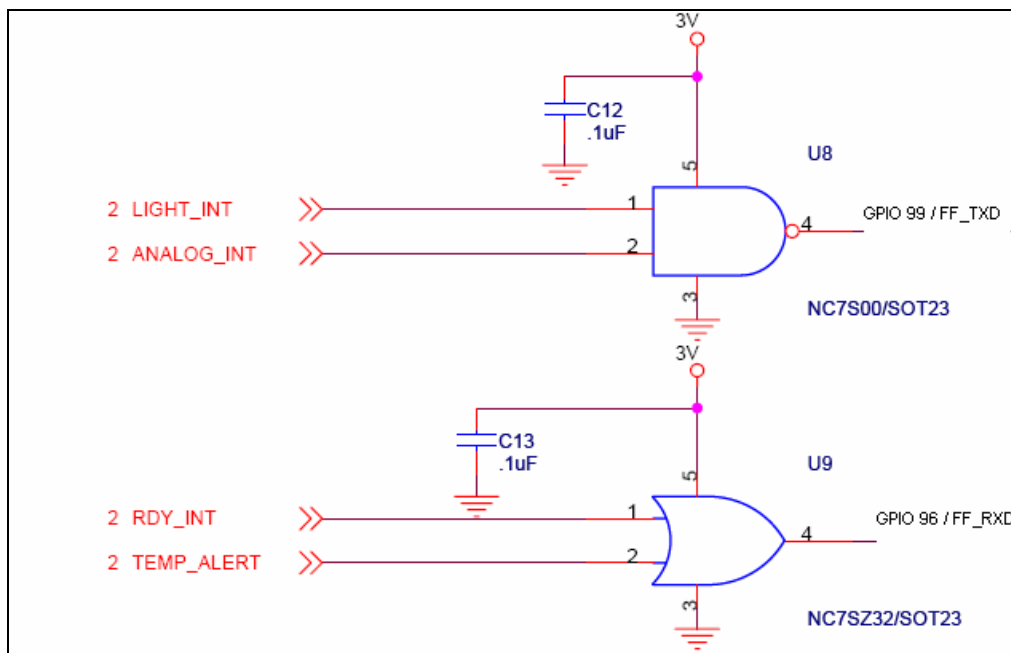
7.1.2 Temperature and Humidity Sensor

The boards include a Sensirion SHT15 sensor which can be used for applications requiring high accuracy temp reading (+/- 0.3 degC) and humidity. This sensor interfaces to the Intel Mote 2 through two GPIO pins. The data pin of the SHT11 is connected to GPIO 100, whereas the clock pin is connected to GPIO 98. Another set of connections is available by loading R36 and R37 if no conflict exists with another stacked board. For more information on the SHT11 sensor, please reference its datasheet located at: http://www.sensirion.com/images/getFile?id=25

7.1.3 Light Sensor

The board includes a TAOS TSL2651 light sensor. This sensor interfaces to the Intel Mote 2 through the I2C bus. The interrupt pin (LIGHT_INT) is connected to GPIO99 through a NAND gate as shown in the schematic above. If another board conflicts with the use of GPIO 99, the BT_TXD pin can be used instead by loading R35.   The address select line is driven by R4 and R6 and is set to 1 by default (R4 in, R6 out). To set it to 0, populate R6 and remove R4. To float it, remove both R4 and R6. Refer to data sheet for address mapping. The data sheet can be found at http://www.taosinc.com/product_detail.asp?cateid=4&proid=60

7.1.4 General purpose A/D

The board includes a Maxim MAX1363, 4 channel, 12 bit resolution general purpose ADC for quick prototyping. Each channel supports 0-3 V input signals. The ADC interfaces to the Intel Mote 2 through the I2C bus. The analog pins are brought out to a Molex PN-39357-0003 connector (J5) and the pin assignment is shown below.   Pin A0 which controls the I2C address of the ADC is driven to 0 by default (R7 out, R9 in). If the I2C address needs to be changed, A0 can be driven to 1 (as specified in the data sheet) by removing R9 and populating R7.

The interrupt line (ANALOG_INT) is connected to GPIO99 through a NAND gate as shown in schematic above. If another board conflicts with the use of GPIO 99, the BT_TXD pin can be used instead by loading R35. The datasheet can be found at http://pdfserv.maxim-ic.com/en/ds/MAX1363-MAX1364.pdf.

7.1.5 Digital Temperature Sensor with two wire interface

The board includes a TI TMP175, a digital temperature sensor with a two wire output serial interface. The device is capable of a $\pm 1.5°C$ accurate over the range of -25°C to +85°C. The sensor allows up to 27 I2C devices on the bus. TMP175 address can be configured via resistors R13,R14,R15,R16,R27,R28. See schematic and TMP175 datasheet for more details. The interrupt line(TEMP_ALERT) is connected to GPIO96(FF_TXD) as shown in the schematic above. The datasheet for the device can be found at http://focus.ti.com/lit/ds/symlink/tmp175.pdf

7.2 Boost Switcher and Linear Regulator

The board includes a switching voltage regulator (U11-LTC3426), followed by linear regulator (U12-LTC1962). The input to the boost regulator is provided from the battery. In order to provide a cleaner power supply the output of the switcher is regulated further with a linear regulator. Regulated voltage output is provided externally through the connector J5 pin 5. It could be used for prototyping purposes in the case where a user of the board requires a voltage that is higher than anything provided by the board. All boards are shipped with the switcher/regulator disabled. See schematic and datasheet details on how to enable the switcher and set the voltages on both the switcher and the regulator.

7.3 Communication and Addressing

The Light Sensor (U2), Simple Temp Sensor (U7) and general purpose A/D (U1) can only be accessed via the I2C bus. Resistor settings control device addressing.

Table 7-2. ITS400 Default I2C addresses

Sensor	Address
TS2561(U2)	1001001
TMP175(U7)	1001010
MAX1363(U1)	0110100

◄ **NOTE:**

Temp Sensor (U6) is not I2C compatible and utilizes a proprietary serial communication protocol. Please see its datasheet for more information.
3D Accelerometer can be configured to communicate over either I2C or SPI serial buses.
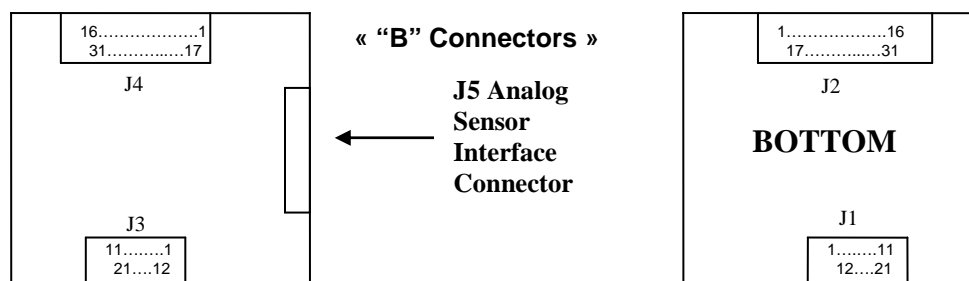
7.4 Pin-out Description

```
16..................1                               1..................16
31..............17          « "B" Connectors »      17..............31
      J4                                                  J2
                            J5 Analog
                         ←  Sensor                      BOTTOM
                            Interface
                            Connector
      J3                                                  J1
11........1                                         1........11
21....12                                            12....21
```

Table 7-3. ITS400 Pin-out description for Small "A" connector

Pin #	Type	Name	Description
A1[1]	PWR	VBAT	Not used by the sensor board, serves as input to the switcher
A2[1]	PWR	VBAT	Not used by the sensor board, serves as input to the switcher
A3		GND	Ground
A4[1]	PWR	PMIC_TBAT	Not used by the sensor board
A5	*R*	*Reserved*	*Do not connect*
A6	*R*	*Reserved*	*Do not connect*
A7	*R*	*Reserved*	*Do not connect*
A8	*R*	*Reserved*	*Do not connect*
A9	*R*	*Reserved*	*Do not connect*
A10	*R*	*Reserved*	*Do not connect*
A11	*R*	*Reserved*	*Do not connect*
A12[1]	PWR	1.8V	Not used by the sensor board
A13[1]	PWR	3.0V	Sensor Board Power Supply
A14[1]	*R*	*Reserved*	*Do not connect*
A15[1]		Alarm	Not used by the sensor board
A16[1]		Reset	Not used by the sensor board
A17		*GND*	*Ground*
A18[1]		VRTC	Not used by the sensor board
A19[1]		nCHARGE_EN	Not used by the sensor board
A20[1]		STD_RXD	Not used by the sensor board
A21[1]		STD_TXD	Not used by the sensor board

---

[1] Passed through to the bottom connectors J3 & J4 on the same pins.

Table 7-4. ITS400 Pin-out description Large "B" connector

Pin #	Type	Name	Description
B1	O	FF_RXD	Logical OR of RDY_INT and TEMP_ALERT(Note1.1)
B2	O	FF_TXD	Logical NAND of LIGHT_INT and ANALOG_INT(Note1.2)
B3	I/O	FF_CTS	Serial Data for SHT15
B4	I	FF_RTS	Serial Clock for SHT15
B5[1]		BT_RXD	An alternative connection to B1
B6[1]		BT_TXD	An alternative connection to B2
B7[1]		BT_CTS	An alternative connection to B3
B8[1]		BT_RTS	An alternative connection to B4
B9		GND	Ground
B10[1]		SSP2_SCLK	An alternative connection to B19
B11[1]		*SSP2_SFRM*	An alternative connection to B20
B12[1]		SSP2_TXD	An alternative connection to B21
B13[1]		SSP2_RXD	An alternative connection to B22
B14[1]		GPIO_94	Not used by the sensor board
B15	*R*	*RFU8*	*Do not connect*
B16	*R*	*RFU9*	*Do not connect*
B17[1]	I	I2C_SCL/SCL_SPC	I2C Clock/SPI Serial Port Clock
B18[1]	I/O	I2C_SDA/SDL_SDI_SDO	I2C Data/SPI Serial Data Input
B19[1]	I/O	SSP1_SCLK/SCL_SPC	SPI serial clock
B20[1]	I	SSP1_SFRM/SPI_CS	SPI chip select
B21[1]	I	SSP1_TXD/SDA_SDI_SDO	SPI serial data input for accelerometer
B22[1]	O	SSP1_RXD/SDO	SPI serial data output for accelerometer
B23[1]		GPIO10	Not used by the sensor board
B24		GND	Ground
B25[1]		MM_CLK	Not used by the sensor board
B26[1]		MM_CMD	Not used by the sensor board
B27[1]		MM_DATA0	Not used by the sensor board
B28[1]		MM_DATA1	Not used by the sensor board
B29[1]		MM_DATA2	Not used by the sensor board
B30[1]		MM_DATA3	Not used by the sensor board
B31		GPIO_93	Not used by the sensor board

Table 7-5. ITS400 Pin-out description J5-Analog Sensor Interface Connector

Pin #	Type	Name	Description
1	Analog Input	AIN0	Input to an ADC
2	Analog Input	AIN1	Input to an ADC
3	Analog Input	AIN2	Input to an ADC
4	Analog Input	AIN3	Input to an ADC
5	PWR	3V	Switcher/Regulator output supplied from the Sensor Board
6	GND	GND	Ground
7	I/O	I2C SDA	I2C Data
8	I/O	I2C SCL	I2C Clock

7.5 Hardware Errata (Board Rev 2.0)

U7(TMP175) TEMP_ALERT signal requires a 10Kohm pull up to 3V. It's missing in the current revision.

U2(TSL2561) LIGHT_INT signal requires a 10Kohm pull up to 3V. It's missing in the current revision.

8 IIB2400 Interface Board

The IIB2400 interface board is used for code loading and debugging through JTAG. It connects to the Imote2 through the advanced connectors, and is a pass through board to enable debugging with other power/battery boards attached to the Imote2.

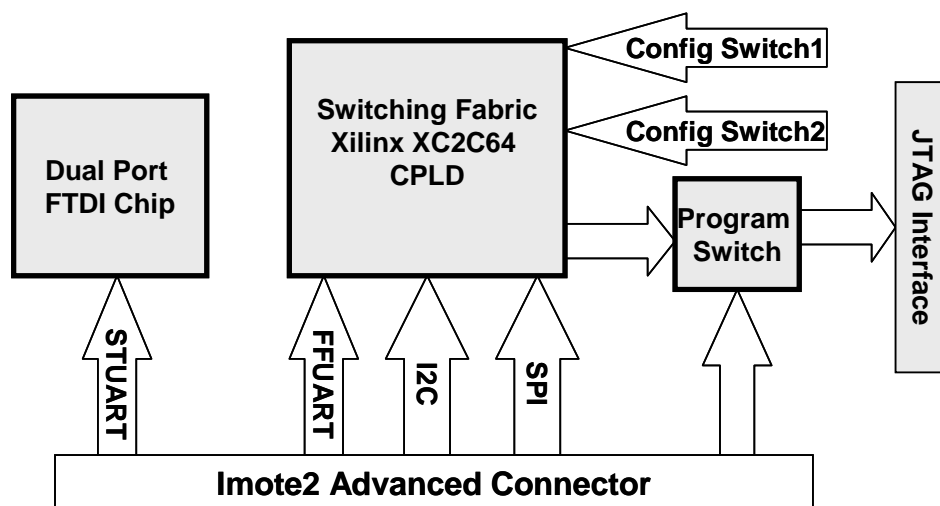**Figure 8-1. Photo of the IIB2400 Interface Board**

Figure 8-2. ITS400 Block diagram

It contains a dual port FTDI chip, mapping the USB input to 2 serial ports. The first serial port connects to the STDUART on the Imote2 platform and is meant to be used for the console. The second serial port can be configured to connect to FFUART regular, FFUART crossover, I2C or

SSP1 ports. This mapping is controlled by the SW5 switch on the board and is labeled accordingly.

The power supply can be controlled by the SW6 switch to select on of the following options:

- Option 1 : USB power drives VBAT to power the mote (marked as "PWR")
- Option 2 : VBAT is not driven (marked as "No PWR")

The debug board is designed to work with both the Intel JTAG dongle and the Macgraigor Raven dongle. It provides the ability to program the mote as well as the on-board CPLD through JTAG. The desired JTAG chain is selected via the SW3 switch.

8.1 Connector Description

```
┌─────────────────────────┐        ┌─────────────────────────┐
│          J3             │        │          J4             │
│   ┌─────────────────┐   │        │   ┌─────────────────┐   │
│   │ 1..............20 │   │        │   │ 20..............1 │   │
│   │ 21.............40 │   │        │   │ 40.............21 │   │
│   └─────────────────┘   │        │   └─────────────────┘   │
│                         │        │                         │
│                         │        │                         │
│    ┌────────────┐       │        │    ┌────────────┐       │
│    │ 1.......10 │       │        │    │ 10.......1 │       │
│    │ 11.....20 │       │        │    │ 20.....11 │       │
│    └────────────┘       │        │    └────────────┘       │
│          J1             │        │          J2             │
└─────────────────────────┘        └─────────────────────────┘
          TOP                               Bottom
```
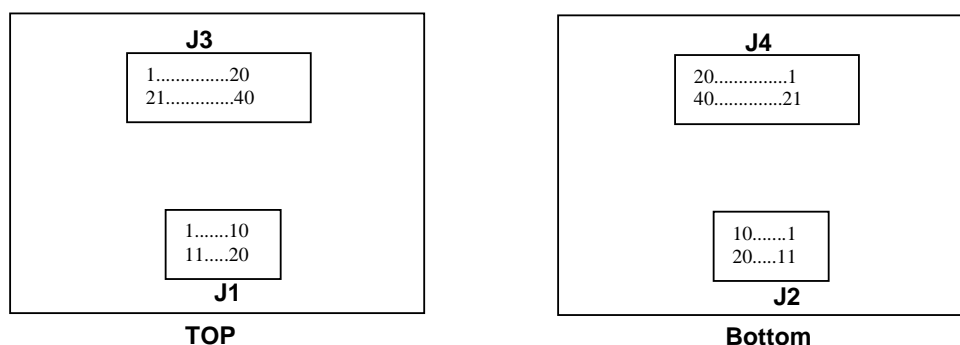
Table 8-1. Connector information

Description	Manufacturer	Part #
40 pin Advanced (J3)	Hirose	DF15B(1.8)-40DP-0.65V(50)
20 pin Advanced (J1)	Hirose	DF15B(1.8)-20DP-0.65V(50)
40 pin Advanced (J4)	Hirose	DF15B(1.8)-40DS-0.65V(50)
20 pin Advanced (J2)	Hirose	DF15B(1.8)-20DS-0.65V(50)

9 Appendix A. Warranty and Support Information

9.1 Customer Service

As a Crossbow Technology customer you have access to product support services, which include:

- Single-point return service
- Web-based support service
- Same day troubleshooting assistance
- Worldwide Crossbow representation
- Onsite and factory training available
- Preventative maintenance and repair programs
- Installation assistance available

9.2 Contact Directory

United States: Phone: 1-408-965-3300 (8 AM to 5 PM PST)

Fax: 1-408-324-4840 (24 hours)

Email: techsupport@xbow.com

Non-U.S.: refer to website   www.xbow.com

9.3 Return Procedure

9.3.1 Authorization

Before returning any equipment, please contact Crossbow to obtain a Returned Material Authorization number (RMA).

Be ready to provide the following information when requesting a RMA:

- Name
- Address
- Telephone, Fax, Email
- Equipment Model Number
- Equipment Serial Number
- Installation Date
- Failure Date
- Fault Description

9.3.2 Identification and Protection

If the equipment is to be shipped to Crossbow for service or repair, please attach a tag TO THE EQUIPMENT, as well as the shipping container(s), identifying the owner. Also indicate the service or repair required, the problems encountered and other information considered valuable to the service facility such as the list of information provided to request the RMA number.

Place the equipment in the original shipping container(s), making sure there is adequate packing around all sides of the equipment. If the original shipping containers were discarded, use heavy boxes with adequate padding and protection.

9.3.3 Sealing the Container

Seal the shipping container(s) with heavy tape or metal bands strong enough to handle the weight of the equipment and the container.

9.3.4 Marking

Please write the words, "*FRAGILE, DELICATE INSTRUMENT*" in several places on the outside of the shipping container(s). In all correspondence, please refer to the equipment by the model number, the serial number, and the RMA number.

9.3.5 Return Shipping Address

Use the following address for all returned products:

Crossbow Technology, Inc.
  4145 N. First Street
  San Jose, CA 95134
  Attn: RMA Number (XXXXXX)

9.4 Warranty

The Crossbow product warranty is one year from date of shipment.

TMP175
TMP75

Digital Temperature Sensor
with Two-Wire Interface

FEATURES

- **27 ADDRESSES (TMP175)**
  8 ADDRESSES (TMP75)
- **DIGITAL OUTPUT: Two-Wire Serial Interface**
- **RESOLUTION: 9- to 12-Bits, User-Selectable**
- **ACCURACY:**
  ±1.5°C (max) from –25°C to +85°C
  ±2.0°C (max) from –40°C to +125°C
- **LOW QUIESCENT CURRENT:**
  50µA, 0.1µA Standby
- **WIDE SUPPLY RANGE: 2.7V to 5.5V**
- **SMALL SO-8 AND MSOP-8 PACKAGES**

APPLICATIONS

- **POWER-SUPPLY TEMPERATURE MONITORING**
- **COMPUTER PERIPHERAL THERMAL PROTECTION**
- **NOTEBOOK COMPUTERS**
- **CELL PHONES**
- **BATTERY MANAGEMENT**
- **OFFICE MACHINES**
- **THERMOSTAT CONTROLS**
- **ENVIRONMENTAL MONITORING AND HVAC**
- **ELECTROMECHANICAL DEVICE TEMPERATURE**

DESCRIPTION

The TMP175 and TMP75 are two-wire, serial output temperature sensors available in SO-8 and MSOP-8 packages. Requiring no external components, the TMP175 and TMP75 are capable of reading temperatures with a resolution of 0.0625°C.

The TMP175 and TMP75 feature a Two-Wire interface that is SMBus-compatible, with the TMP175 allowing up to 27 devices on one bus and the TMP75 allowing up to eight devices on one bus. The TMP175 and TMP75 both feature an SMBus Alert function.

The TMP175 and TMP75 are ideal for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.

The TMP175 and TMP75 are specified for operation over a temperature range of –40°C to +125°C.
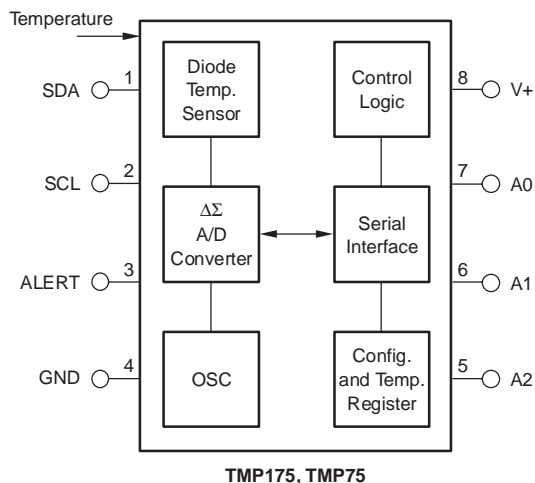
TMP175, TMP75

TEXAS INSTRUMENTS
www.ti.com

TMP175
TMP75

SBOS288J – JANUARY 2004 – REVISED DECEMBER 2007

TEXAS
INSTRUMENTS
www.ti.com

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply, V+	7.0V
Input Voltage[2]	–0.5V to 7.0V
Input Current	10mA
Operating Temperature Range	–55°C to +127°C
Storage Temperature Range	–60°C to +130°C
Junction Temperature (T_J max)	+150°C
ESD Rating:	
Human Body Model (HBM)	4000V
Charged Device Model (CDM)	1000V
Machine Model (MM)	300V

[1] Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

[2] Input voltage rating applies to all TMP175 and TMP75 input voltages.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
TMP175	SO-8	D	TMP175
TMP175	MSOP-8	DGK	DABQ
TMP75	SO-8	D	TMP75
TMP75	MSOP-8	DGK	T127

[1] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN ASSIGNMENTS

Top View
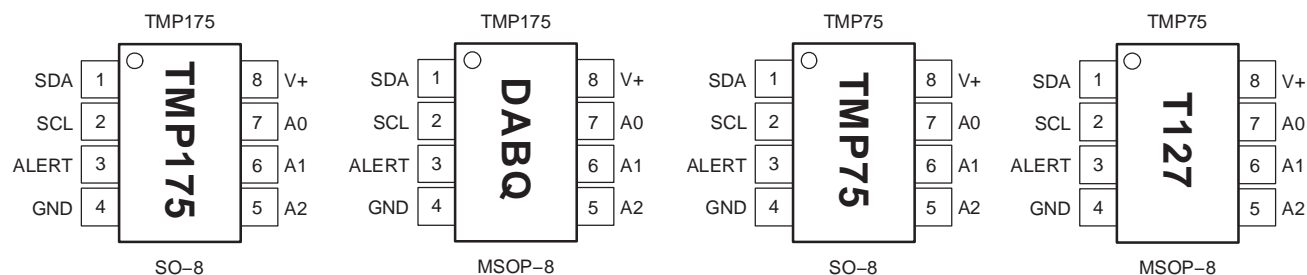
NOTE: Pin 1 is determined by orienting the package marking as indicated in the diagram.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +125°C, and V+ = 2.7V to 5.5V, unless otherwise noted.

PARAMETER	CONDITION	TMP175 MIN	TMP175 TYP	TMP175 MAX	TMP75 MIN	TMP75 TYP	TMP75 MAX	UNITS
TEMPERATURE INPUT								
Range		–40		+125	–40		+125	°C
Accuracy (Temperature Error)	–25°C to +85°C		±0.5	±1.5		±0.5	±2.0	°C
	–40°C to +125°C		±1.0	±2.0		±1.0	±3.0	°C
vs Supply			0.2	±0.5		0.2	±0.5	°C/V
Resolution[1]	Selectable		+0.0625			+0.0625		°C
DIGITAL INPUT/OUTPUT								
Input Capacitance			3			3		pF
Input Logic Levels:								
V_{IH}		0.7(V+)		6.0	0.7(V+)		6.0	V
V_{IL}		–0.5		0.3(V+)	–0.5		0.3(V+)	V
Leakage Input Current, I_{IN}	0V ≤ V_{IN} ≤ 6V			1			1	µA
Input Voltage Hysteresis	SCL and SDA Pins		500			500		mV
Output Logic Levels:								
V_{OL} SDA	I_{OL} = 3mA	0	0.15	0.4	0	0.15	0.4	V
V_{OL} ALERT	I_{OL} = 4mA	0	0.15	0.4	0	0.15	0.4	V
Resolution	Selectable		9 to 12			9 to 12		Bits
Conversion Time	9-Bit		27.5	37.5		27.5	37.5	ms
	10-Bit		55	75		55	75	ms
	11-Bit		110	150		110	150	ms
	12-Bit		220	300		220	300	ms
Timeout Time		25	54	74	25	54	74	ms
POWER SUPPLY								
Operating Range		2.7		5.5	2.7		5.5	V
Quiescent Current I_Q	Serial Bus Inactive		50	85		50	85	µA
	Serial Bus Active, SCL Freq = 400kHz		100			100		µA
	Serial Bus Active, SCL Freq = 3.4MHz		410			410		µA
Shutdown Current I_{SD}	Serial Bus Inactive		0.1	3		0.1	3	µA
	Serial Bus Active, SCL Freq = 400kHz		60			60		µA
	Serial Bus Active, SCL Freq = 3.4MHz		380			380		µA
TEMPERATURE RANGE								
Specified Range		–40		+125	–40		+125	°C
Operating Range		–55		+127	–55		+127	°C
Thermal Resistance θ_{JA}								
MSOP-8			250			250		°C/W
SO-8			150			150		°C/W

[1] Specified for 12-bit resolution.

TMP175
TMP75

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TYPICAL CHARACTERISTICS

At T_A = +25°C and V+ = 5.0V, unless otherwise noted.

QUIESCENT CURRENT vs TEMPERATURE

V+ = 5V

V+ = 2.7V

Serial Bus Inactive

I_Q (μA) vs Temperature (°C)
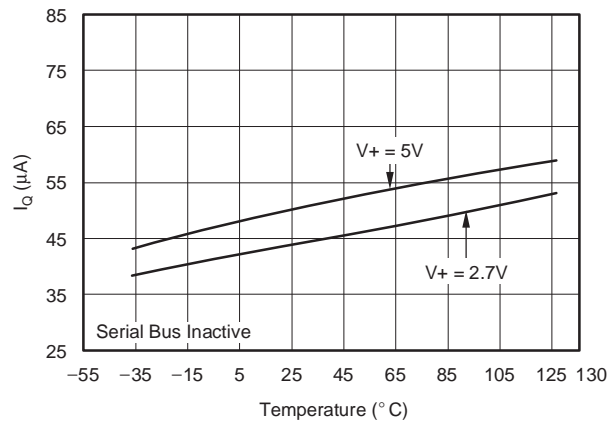
SHUTDOWN CURRENT vs TEMPERATURE

I_{SD} (μA) vs Temperature (°C)
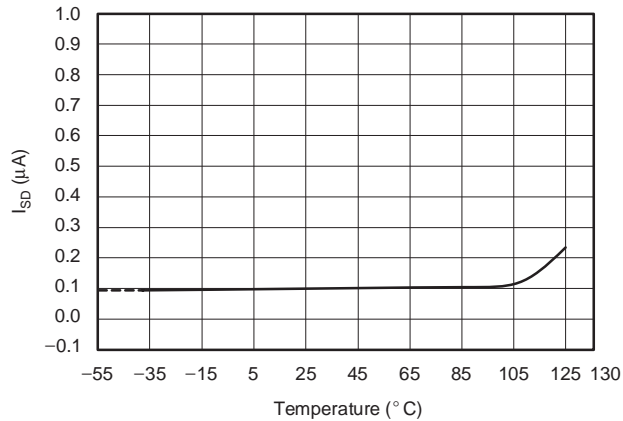
CONVERSION TIME vs TEMPERATURE

V+ = 5V

V+ = 2.7V

12–bit resolution.

Conversion Time (ms) vs Temperature (°C)
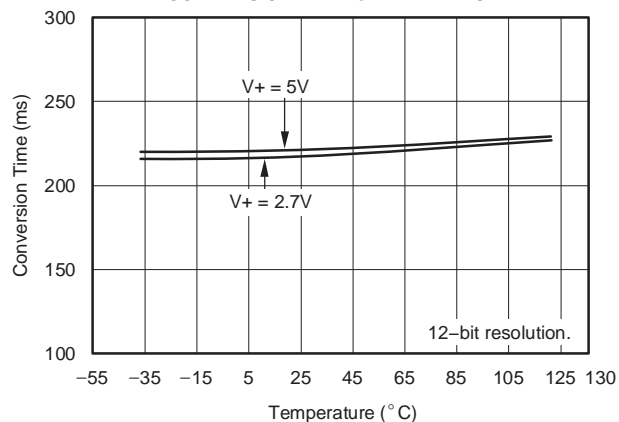
TEMPERATURE ACCURACY vs TEMPERATURE

3 typical units 12–bit resolution.

Temperature Error (°C) vs Temperature (°C)
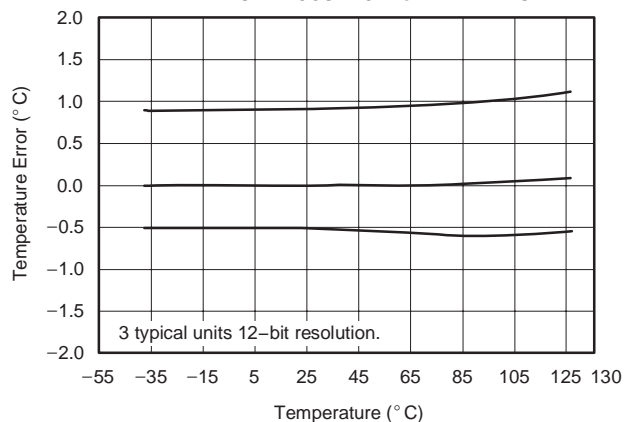
QUIESCENT CURRENT WITH
BUS ACTIVITY vs TEMPERATURE

Hs MODE
FAST MODE

125°C

25°C

−55°C

I_Q (μA) vs Frequency (Hz)
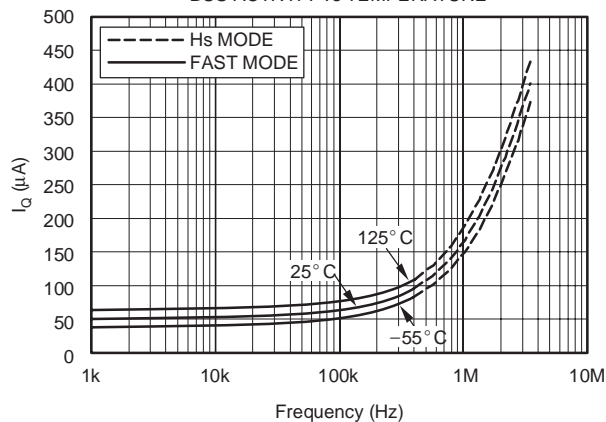
APPLICATIONS INFORMATION

The TMP175 and TMP75 are digital temperature sensors that are optimal for thermal management and thermal protection applications. The TMP175 and TMP75 are Two-Wire and SMBus interface-compatible, and are specified over a temperature range of −40°C to +125°C.

The TMP175 and TMP75 require no external components for operation except for pull-up resistors on SCL, SDA, and ALERT, although a 0.1μF bypass capacitor is recommended, as shown in Figure 1.
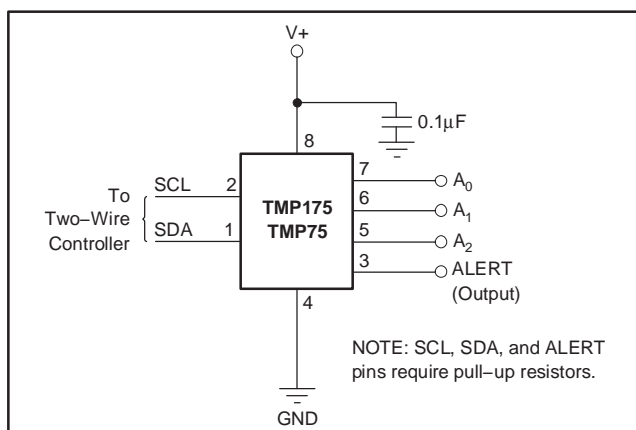
Figure 1. Typical Connections of the TMP175 and TMP75

The sensing device of the TMP175 and TMP75 is the chip itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

To maintain accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive will assist in achieving accurate surface temperature measurement.

POINTER REGISTER

Figure 2 shows the internal register structure of the TMP175 and TMP75. The 8-bit Pointer Register of the devices is used to address a given data register. The Pointer Register uses the two LSBs to identify which of the data registers should respond to a read or write command. Table 1 identifies the bits of the Pointer Register byte. Table 2 describes the pointer address of the registers available in the TMP175 and TMP75. Power-up reset value of P1/P0 is 00.
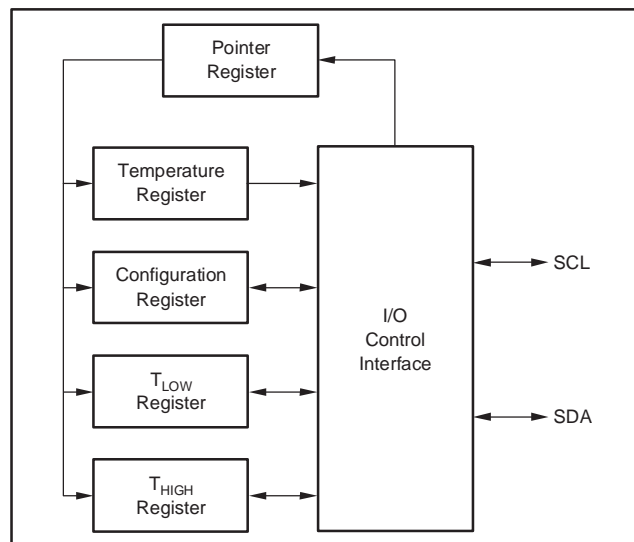
Figure 2. Internal Register Structure of the TMP175 and TMP75

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

Table 1. Pointer Register Byte

P1	P0	REGISTER
0	0	Temperature Register (READ Only)
0	1	Configuration Register (READ/WRITE)
1	0	T_{LOW} Register (READ/WRITE)
1	1	T_{HIGH} Register (READ/WRITE)

Table 2. Pointer Addresses of the TMP175 and TMP75

TEMPERATURE REGISTER

The Temperature Register of the TMP175 or TMP75 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 3 and Table 4. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Data format for temperature is summarized in Table 5. Following power-up or reset, the Temperature Register will read 0°C until the first conversion is complete.

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Table 3. Byte 1 of Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

Table 4. Byte 2 of Temperature Register

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
−0.25	1111 1111 1100	FFC
−25	1110 0111 0000	E70
−55	1100 1001 0000	C90

Table 5. Temperature Data Format

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration Register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits in the Temperature Register are used with the unused LSBs set to zero.

CONFIGURATION REGISTER

The Configuration Register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format of the Configuration Register for the TMP175 and TMP75 is shown in Table 6, followed by a breakdown of the register bits. The power-up/reset value of the Configuration Register is all bits equal to 0.

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD

Table 6. Configuration Register Format

SHUTDOWN MODE (SD)

The Shutdown Mode of the TMP175 and TMP75 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than $0.1\mu A$. Shutdown Mode is enabled when the SD bit is 1; the device will shut down once the current conversion is completed. When SD is equal to 0, the device will maintain a continuous conversion state.

THERMOSTAT MODE (TM)

The Thermostat Mode bit of the TMP175 and TMP75 indicates to the device whether to operate in Comparator Mode (TM = 0) or Interrupt Mode (TM = 1). For more information on comparator and interrupt modes, see the *High and Low Limit Registers* section.

POLARITY (POL)

The Polarity Bit of the TMP175 and TMP75 allows the user to adjust the polarity of the ALERT pin output. If POL = 0, the ALERT pin will be active LOW, as shown in Figure 3. For POL = 1, the ALERT pin will be active HIGH, and the state of the ALERT pin is inverted.
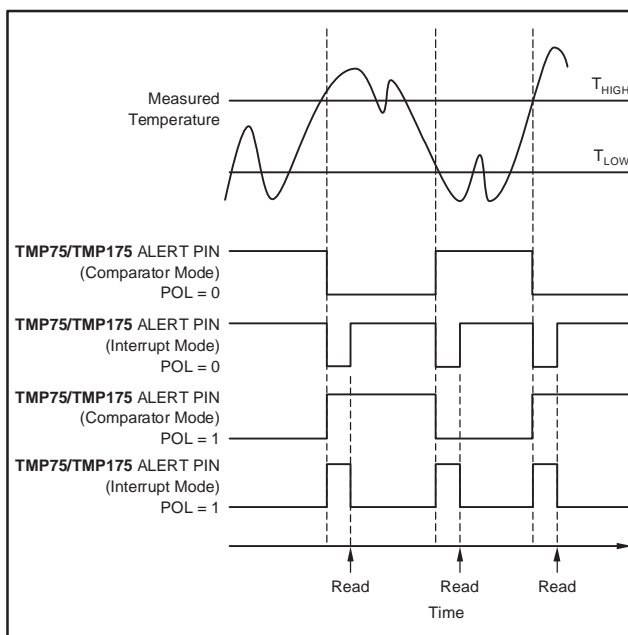
Figure 3. Output Transfer Function Diagrams

FAULT QUEUE (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} Registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 7 defines the number of measured faults that may be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see the section *High and Low Limit Registers*.

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

Table 7. Fault Settings of the TMP175 and TMP75

CONVERTER RESOLUTION (R1/R0)

The Converter Resolution Bits control the resolution of the internal Analog-to-Digital (A/D) converter. This allows the user to maximize efficiency by programming for higher

resolution or faster conversion time. Table 8 identifies the Resolution Bits and the relationship between resolution and conversion time.

R1	R0	RESOLUTION	CONVERSION TIME (typical)
0	0	9 Bits (0.5°C)	27.5ms
0	1	10 Bits (0.25°C)	55ms
1	0	11 Bits (0.125°C)	110ms
1	1	12 Bits (0.0625°C)	220ms

Table 8. Resolution of the TMP175 and TMP75

ONE-SHOT (OS)

The TMP175 and TMP75 feature a One-Shot Temperature Measurement Mode. When the device is in Shutdown Mode, writing a '1' to the OS bit will start a single temperature conversion. The device will return to the shutdown state at the completion of the single conversion. This is useful to reduce power consumption in the TMP175 and TMP75 when continuous temperature monitoring is not required. When the configuration register is read, the OS will always read zero.

HIGH AND LOW LIMIT REGISTERS

In Comparator Mode (TM = 0), the ALERT pin of the TMP175 and TMP75 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin will remain active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt Mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus Alert Response Address. The ALERT pin will also be cleared if the device is placed in Shutdown Mode. Once the ALERT pin is cleared, it will only become active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin will become active and remain active until cleared by a read operation of any register or a successful response to the SMBus Alert Response Address. Once the ALERT pin is cleared, the above cycle will repeat, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This will also clear the state of the internal registers in the device returning the device to Comparator Mode (TM = 0).

Both operational modes are represented in Figure 3. Table 9 and Table 10 describe the format for the T_{HIGH} and T_{LOW} registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and T_{LOW} are:

$$T_{HIGH} = 80°C \text{ and } T_{LOW} = 75°C$$

The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	H3	H2	H1	H0	0	0	0	0

Table 9. Bytes 1 and 2 of T_{HIGH} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	L3	L2	L1	L0	0	0	0	0

Table 10. Bytes 1 and 2 of T_{LOW} Register

All 12 bits for the Temperature, T_{HIGH}, and T_{LOW} registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

SERIAL INTERFACE

The TMP175 and TMP75 operate only as slave devices on the Two-Wire bus and SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP175 and TMP75 both support the transmission protocol for fast (1kHz to 400kHz) and high-speed (1kHz to 3.4MHz) modes. All data bytes are transmitted MSB first.

SERIAL BUS ADDRESS

To communicate with the TMP175 and TMP75, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The TMP175 features three address pins to allow up to 27 devices to be addressed on a single bus interface. Table 11 describes the pin logic levels used to properly connect up to 27 devices. '1' indicates the pin is connected to the supply (V_{CC}); '0' indicates the pin is connected to GND; *Float* indicates the pin is left unconnected. The state of pins A0, A1, and A2 is sampled on every bus communication and should be set prior to any activity on the interface.

The TMP75 features three address pins allowing up to eight devices to be connected per bus. Pin logic levels are described in Table 12. The address pins of the TMP175 and TMP75 are read after reset, at start of communication, or in response to a Two-Wire address acquire request. Following reading the state of the pins the address is latched to minimize power dissipation associated with detection.

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111
Float	0	0	1110000
Float	0	Float	1110001
Float	0	1	1110010
Float	1	0	1110011
Float	1	Float	1110100
Float	1	1	1110101
Float	Float	0	1110110
Float	Float	1	1110111
0	Float	0	0101000
0	Float	1	0101001
1	Float	0	0101010
1	Float	1	0101011
0	0	Float	0101100
0	1	Float	0101101
1	0	Float	0101110
1	1	Float	0101111
0	Float	Float	0110101
1	Float	Float	0110110
Float	Float	Float	0110111

Table 11. Address Pins and Slave Addresses for the TMP175

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111

Table 12. Address Pins and Slave Addresses for the TMP75

BUS OVERVIEW

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge Bit. During data transfer SDA must remain stable while SCL is HIGH, as any change in SDA while SCL is HIGH will be interpreted as a control signal.

Once all data has been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH, while SCL is HIGH.

WRITING/READING TO THE TMP175 AND TMP75

Accessing a particular register on the TMP175 and TMP75 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit LOW. Every write operation to the TMP175 and TMP75 requires a value for the Pointer Register. (Refer to Figure 5.)

When reading from the TMP175 and TMP75, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This is accomplished by issuing a slave address byte with the R/$\overline{\text{W}}$ bit LOW, followed by the Pointer Register Byte. No additional data is required. The master can then generate a START condition and send the slave address byte with the R/$\overline{\text{W}}$ bit HIGH to initiate the read command. See Figure 7 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register bytes, as the TMP175 and TMP75 will remember the Pointer Register value until it is changed by the next write operation.

Note that register bytes are sent most-significant byte first, followed by the least significant byte.

SLAVE MODE OPERATIONS

The TMP175 and TMP75 can operate as slave receivers or slave transmitters.

Slave Receiver Mode:

The first byte transmitted by the master is the slave address, with the R/$\overline{\text{W}}$ bit LOW. The TMP175 or TMP75 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer Register. The TMP175 or TMP75 then acknowledges reception of the Pointer Register byte. The next byte or bytes are written to the register addressed by the Pointer Register. The TMP175 and TMP75 will acknowledge reception of each data byte. The master may terminate data transfer by generating a START or STOP condition.

Slave Transmitter Mode:

The first byte is transmitted by the master and is the slave address, with the R/$\overline{\text{W}}$ bit HIGH. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer Register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master may terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

SMBus ALERT FUNCTION

The TMP175 and TMP75 support the SMBus Alert function. When the TMP75 and TMP175 are operating in Interrupt Mode (TM = 1), the ALERT pin of the TMP75 or TMP175 may be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP75 or TMP175 is active, the devices will acknowledge the SMBus Alert command and respond by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte will indicate if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the ALERT condition. This bit will be HIGH if the temperature is greater than or equal to T_{HIGH}. This bit will be LOW if the temperature is less than T_{LOW}. Refer to Figure 8 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command will determine which device will clear its ALERT status. If the TMP75 or TMP175 wins the arbitration, its ALERT pin will become inactive at the completion of the SMBus Alert command. If the TMP75 or TMP175 loses the arbitration, its ALERT pin will remain active.

GENERAL CALL

The TMP175 and TMP75 respond to a Two-Wire General Call address (0000000) if the eighth bit is 0. The device will acknowledge the General Call address and respond to commands in the second byte. If the second byte is 00000100, the TMP175 and TMP75 will latch the status of their address pins, but will not reset. If the second byte is 00000110, the TMP175 and TMP75 will latch the status of their address pins and reset their internal registers to their power-up values.

HIGH-SPEED MODE

In order for the Two-Wire bus to operate at frequencies above 400kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP175 and TMP75 will not acknowledge this byte, but will switch their input filters on SDA and SCL and their output filters on SDA to operate in Hs-mode, allowing transfers at up to 3.4MHz. After the Hs-mode master code has been issued, the master will transmit a Two-Wire slave address to initiate a data transfer operation. The bus will continue to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP175 and TMP75 will switch the input and output filter back to fast-mode operation.

TIMEOUT FUNCTION

The TMP175 and TMP75 will reset the serial interface if either SCL or SDA are held LOW for 54ms (typ) between a START and STOP condition. The TMP175 and TMP75 will release the bus if it is pulled LOW and will wait for a START condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1kHz for SCL operating frequency.

TIMING DIAGRAMS

The TMP175 and TMP75 are Two-Wire and SMBus compatible. Figure 4 to Figure 8 describe the various operations on the TMP175 and TMP75. Bus definitions are given below. Parameters for Figure 4 are defined in Table 13.

Bus Idle: Both SDA and SCL lines remain HIGH.

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge on the last byte that has been transmitted by the slave.

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL Operating Frequency	$f_{(SCL)}$	0.001	0.4	0.001	3.4	MHz
Bus Free Time Between STOP and START Condition	$t_{(BUF)}$	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	100		100		ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$	100		100		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	100		100		ns
Data Hold Time	$t_{(HDDAT)}$	0		0		ns
Data Setup Time	$t_{(SUDAT)}$	100		10		ns
SCL Clock LOW Period	$t_{(LOW)}$	1300		160		ns
SCL Clock HIGH Period	$t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time	t_F		300		160	ns
Clock/Data Rise Time	t_R		300		160	ns
for SCLK ≤ 100kHz	t_R		1000			ns

Table 13. Timing Diagram Definitions for the TMP175 and TMP75

TWO-WIRE TIMING DIAGRAMS
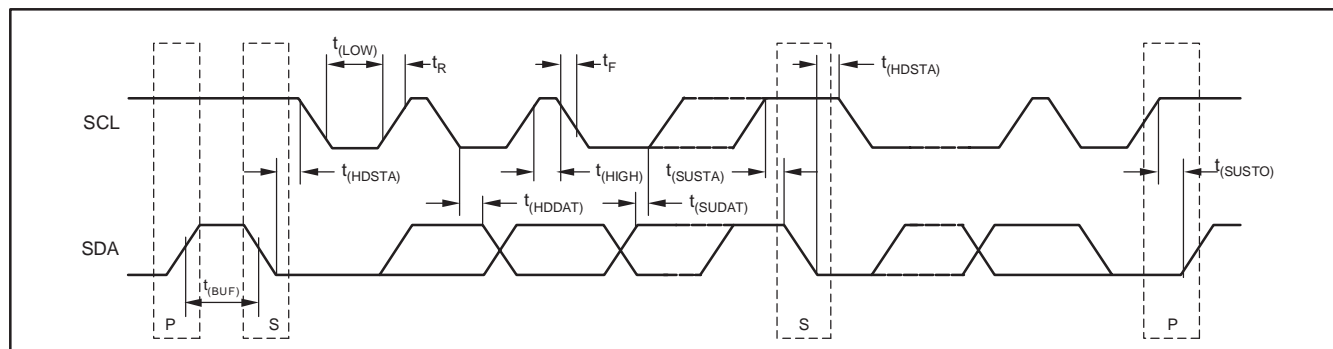
Figure 4. Two-Wire Timing Diagram
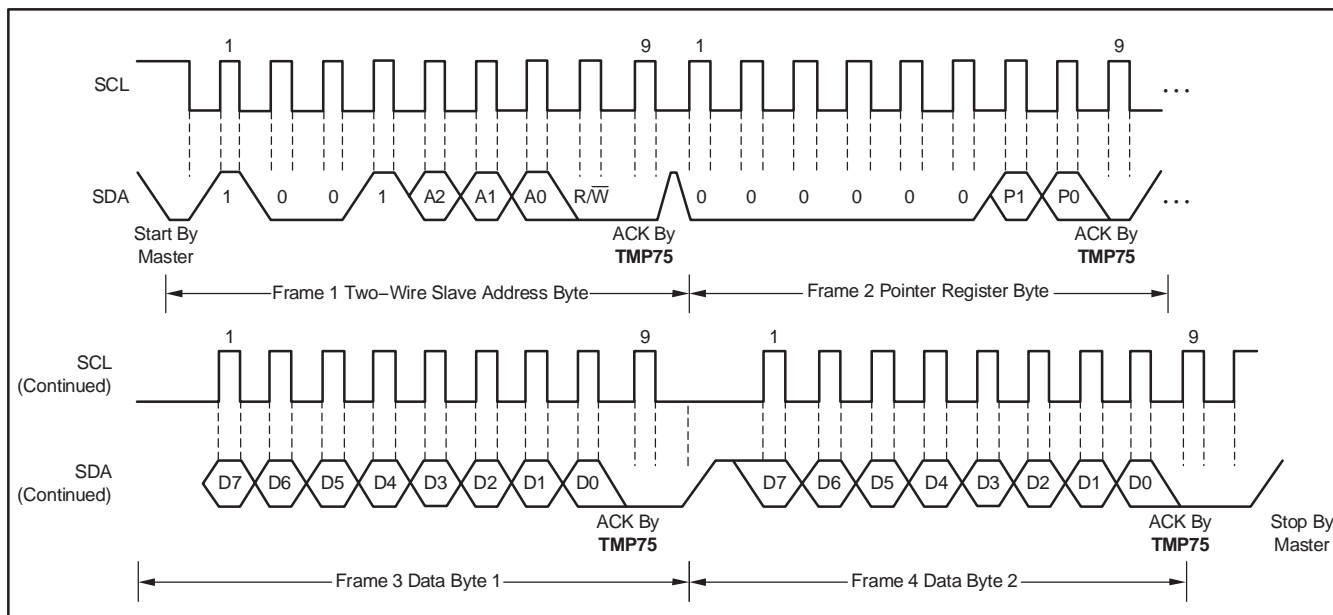
Figure 5. Two-Wire Timing Diagram for TMP75 Write Word Format
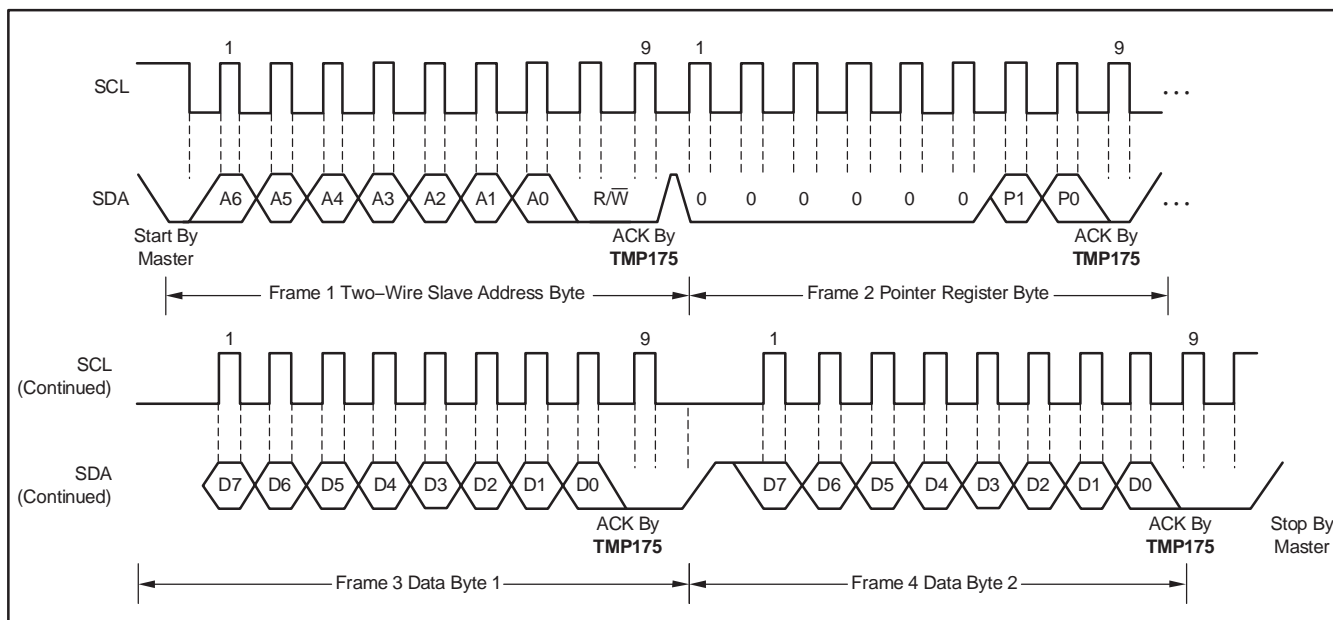
Figure 6. Two-Wire Timing Diagram for TMP175 Write Word Format
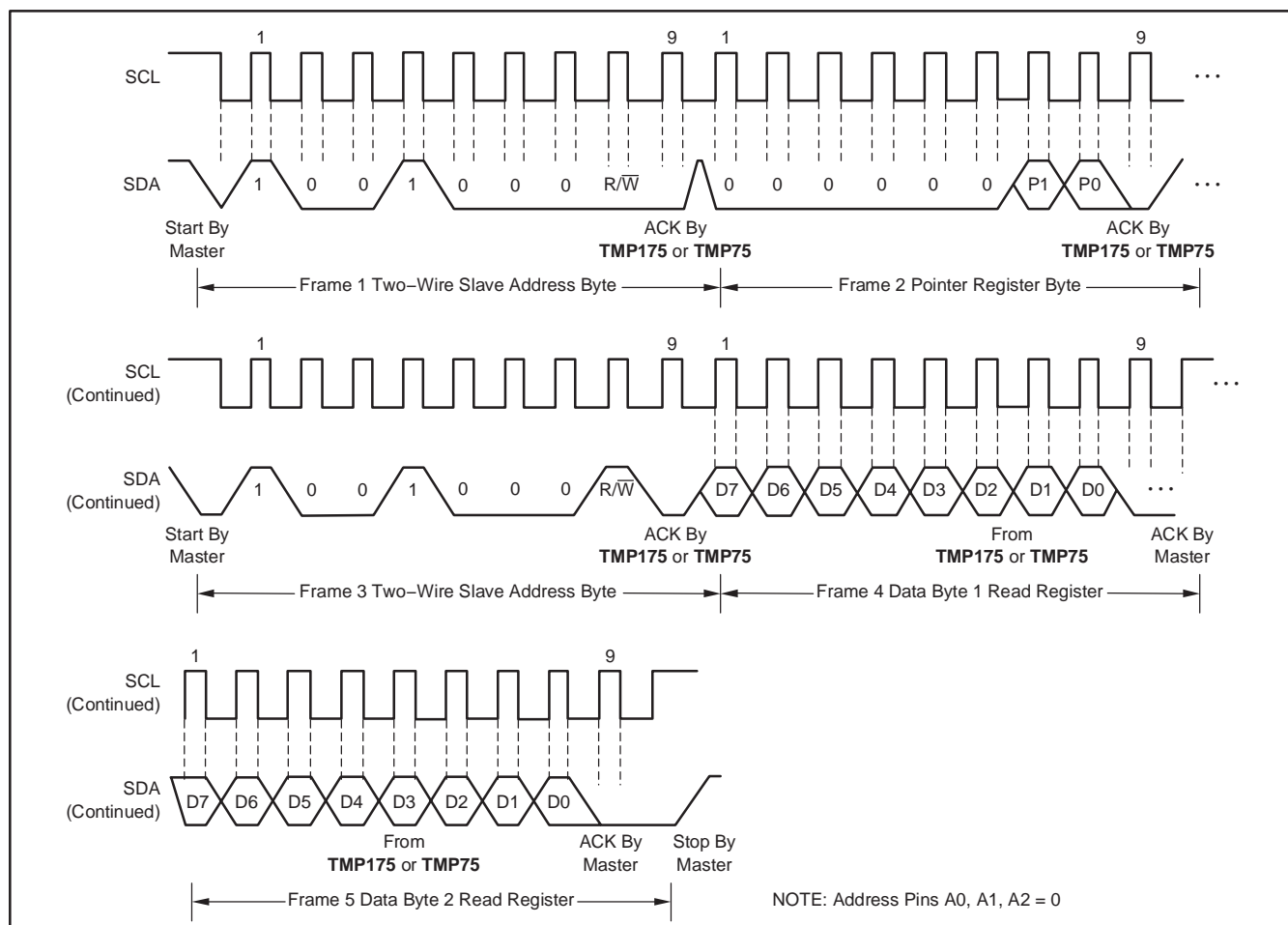
Figure 7. Two-Wire Timing Diagram for Read Word Format
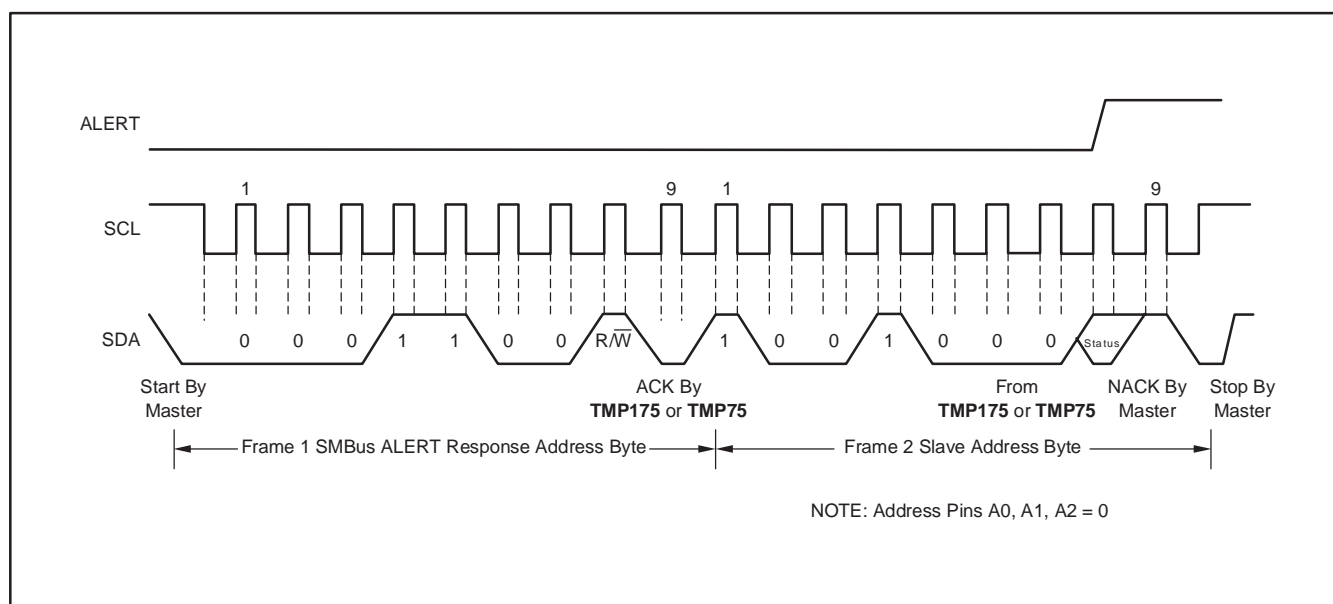
Figure 8. Timing Diagram for SMBus ALERT

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TMP175AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
TMP175AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR
TMP175AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TMP175AIDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TMP175AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TMP175AIDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TMP175AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TMP175AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TMP75AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TMP75AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TMP75AIDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TMP75AIDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TMP75AIDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TMP75AIDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TMP75AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TMP75AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP175AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP175AIDGKT	MSOP	DGK	8	250	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP175AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMP75AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP75AIDGKT	MSOP	DGK	8	250	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP75AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP175AIDGKR	MSOP	DGK	8	2500	370.0	355.0	55.0
TMP175AIDGKT	MSOP	DGK	8	250	370.0	355.0	55.0
TMP175AIDR	SOIC	D	8	2500	346.0	346.0	29.0
TMP75AIDGKR	MSOP	DGK	8	2500	370.0	355.0	55.0
TMP75AIDGKT	MSOP	DGK	8	250	370.0	355.0	55.0
TMP75AIDR	SOIC	D	8	2500	346.0	346.0	29.0

DGK (S−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE

0,65

0,38
0,25   ⊕ 0,13 Ⓜ

8   5

D▷ 3,10
    2,90   5,05
             4,75

1   4
  C▷
3,10
2,90

0,23
0,13

Gauge Plane

0°−8°   0,25

0,70
0,40

1,10 MAX   0,15
              0,05

Seating Plane
          ⌂ 0,10

4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
      C▷ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.15 per end.
      D▷ Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
         E. Falls within JEDEC MO−187 variation AA, except interlead flash.

TEXAS
INSTRUMENTS
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D (R−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE

0.197 (5,00)
0.189 (4,80)
△C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)   △D
0.150 (3,80)

Pin 1
Index Area

1   4

0.050 (1,27)   0.020 (0,51)
                         0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max   0.010 (0,25)
                         0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane   0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−2/I   10/2008
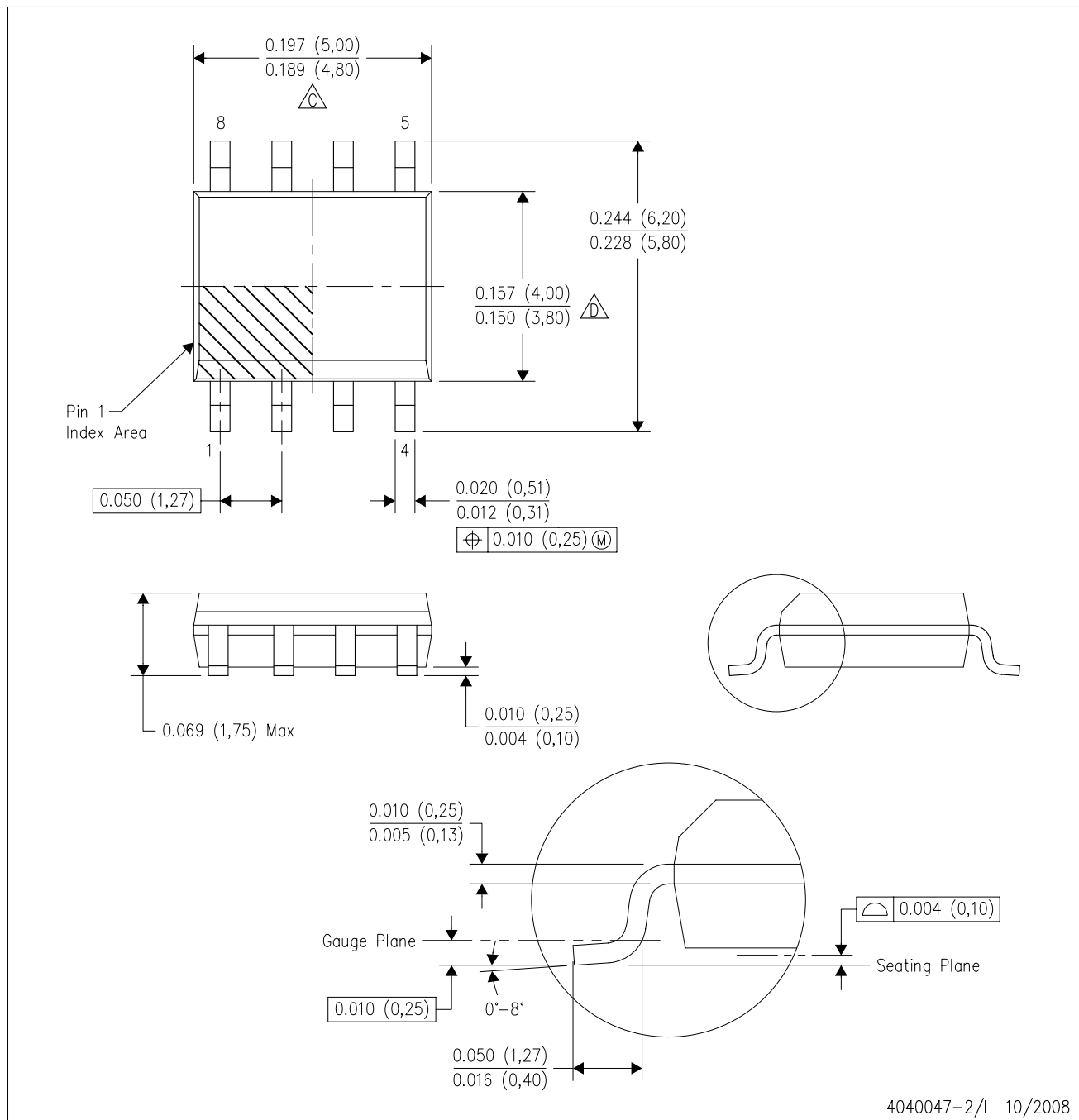
NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
      △C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed .006 (0,15) per end.
      △D.   Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
         E.   Reference JEDEC MS−012 variation AA.